Implementation of a CORDIC based Double-Precision Exponential Core on an FPGA

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Objective:

- High-precision (double precision IEEE 754) e^{-x} core for FPGA
- Small look-up table (so multiple cores can be instantiated without contention for off-chip memory) ability to be pipelined

State-of-the-Art:

- Most implementations described in the literature either compromise precision for speed or
- Use large (unscalable) look-up tables

Approach:

- Started with generic CORDIC algorithm
- Algebraically simplified CORDIC's three equations to two (all that is need for e^{-x})
- Added the ability to compute e^{x} without a floating-point division

Results:

- Very precise (maximum error is 2^{-53} for 10^{10} samples over the range $0 < x < \ln(2)$)
- Modest logic resources 2024 slices (or about 8% of a Virtex 4 XC4VFX60)
- Modest memory resources 3660 bits (or about 457.5 bytes)